What Is Claimed Is:

1. A method for CPU power management and bus optimization for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the following steps:

setting an initial bus bandwidth, an initial bus frequency, a bus operating bandwidth and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus bandwidth and the initial bus frequency;

initializing power management settings of the CPU, the Northbridge and the Southbridge, wherein the CPU operates at a CPU operating frequency with a CPU operating voltage;

obtaining a maximum operating frequency and a maximum operating voltage for the CPU;

outputting a CPU operating frequency and voltage adjustment to the Southbridge according to the maximum operating frequency and the maximum operating voltage;

output of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge, initializing a timer for calculating an elapsed time value;

adjusting the CPU operating frequency and the CPU operating voltage according to CPU operating frequency and voltage adjustment;

output of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; and

reconnection of the CPU and the Northbridge by the bus according to the bus connection signal, wherein the bus operates at the bus operating bandwidth and the bus operating frequency, the CPU operating at the adjusted CPU operating frequency with the adjusted CPU operating voltage according to the CPU operating frequency and voltage adjustment.

2. The method as claimed in claim 1, wherein the bus is a lightning data transport bus.

3. The method as claimed in claim 1, wherein the bus is a hyper-transport bus.

4. The method as claimed in claim 1, wherein the bus disconnection signal and the bus connection signal are output by a single output terminal.

5. A method for CPU power management and bus optimization for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the following steps:

setting an initial bus bandwidth, an initial bus frequency, a bus operating bandwidth and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus bandwidth and the initial bus frequency;

initializing power management setting of the CPU, the Northbridge and the Southbridge, wherein the CPU operates at a first CPU operating frequency with a first CPU operating voltage;

detecting CPU loading and setting a second CPU operating frequency and a second CPU operating voltage according to the detection;

outputting a CPU operating frequency and voltage adjustment to the Southbridge;

output of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge, initializing a timer for calculating an elapsed time value;

output of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; and

reconnection of the CPU and the Northbridge by the bus according to the bus connection signal, wherein the bus operates at the bus operating bandwidth and the bus operating frequency, and the CPU operates at the second CPU operating frequency with the second CPU operating voltage.

6. The method as claimed in claim 5, wherein the bus is a lightning data transport bus.

7. The method as claimed in claim 5, wherein the bus is a hyper-transport bus.

8. The method as claimed in claim 5, wherein the bus disconnection signal and the bus connection signal are output by a single output terminal.

9. The method as claimed in claim 5, further comprising the following steps:

obtaining a maximum operating frequency and a maximum operating voltage of the CPU; and

setting the second CPU operating frequency and the second CPU operating voltage according to the maximum operating frequency and the maximum operating voltage of the CPU.

10. The method as claimed in claim 9, wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge.

11. A method for CPU power management and bus optimization for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the following steps:

setting an initial bus bandwidth, an initial bus frequency, a bus operating bandwidth and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus bandwidth and the initial bus frequency;

initializing power management settings of the CPU, the Northbridge and the Southbridge, wherein the CPU operates at a first CPU operating frequency with a first CPU operating voltage;

obtaining a maximum operating frequency and a maximum operating voltage of the CPU;

detecting the loading on the CPU and setting a second CPU operating frequency and a second CPU operating voltage according to the detection;

outputting a CPU operating frequency and voltage adjustment to the Southbridge according to the maximum operating frequency and the maximum operating voltage;

output of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge, initializing a timer for calculating an elapsed time value;

output of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; and

reconnection of the CPU and the Northbridge by the bus according to the bus connection signal, wherein the bus operates at the bus operating bandwidth and the bus operating frequency, and the CPU operates at the second CPU operating frequency with the second CPU operating voltage.

12. The method as claimed in claim 11, wherein the bus is a lightning data transport bus.

13. The method as claimed in claim 11, wherein the bus is a hyper-transport bus.

14. The method as claimed in claim 11, wherein the bus disconnection signal and the bus connection signal are output by a single output terminal.

15. The method as claimed in claim 14, wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge.